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(71)Applicant : OTSUKA KANJI
USAMI TAMOTSU
HITACHI LTD
OKI ELECTRIC IND CO LTD
SANYO ELECTRIC CO LTD
SHARP CORP
SONY CORP
TOSHIBA CORP
NEC CORP
MATSUSHITA ELECTRIC IND CO LTD
MITSUBISHI ELECTRIC CORP
FUJITSU LTD
ROHM CO LTD

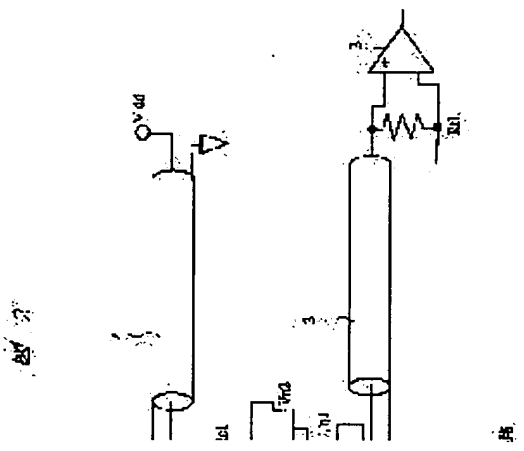
(72)Inventor : OTSUKA KANJI
USAMI TAMOTSU

(54) SIGNAL TRANSMISSION SYSTEM

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a signal transmission technique for transferring a high- speed digital signal of several tens of GHz band, while meeting the conventional system configuration and component configuration, as much as possible.

SOLUTION: In a configuration of a driver 1 and a receiver 2 included in a transistor logic circuit spread over the whole electronic circuit and a memory circuit, a



signal transmission system includes the driver 1, which is connected both to the receiver 2 through a signal transmission line 3 and to a power source Vdd through a power source and ground transmission line 4. Both the driver 1 and the receiver 2 are configured, to have substantially differential inputs and substantially differential outputs, and at the output ends of the substantially differential outputs of the driver 1, connection to the power source is not provided nor to the ground. The receiver 2 receives the signal, by detecting a voltage difference between the substantially differential input signals, and further, the signal transmission line 3 has no distribution wiring.

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CLAIMS

[Claim(s)]
[Claim 1] The logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit, and a receiver circuit, It has the signal-transmission track which connects said driver circuit and said receiver circuit electrically. All of said driver circuit and said receiver circuit are a substantial difference input and a differential output. It is the signal-transmission system characterized by what said receiver circuit is received by detecting the potential difference of the signal of a substantial difference input, and said signal-transmission track does not have distribution wiring for, without having connection with a power source or a gland in the outgoing end of the substantial differential output of said driver circuit.
[Claim 2] It is the signal-transmission system which has an electric power supply line further in a signal-transmission system according to claim 1, and is characterized by what said electric power supply line is the structure used as a power source and the grand pair transmission line, and is connected to per 1 element circuit of each minimum logical element circuit and a memory element circuit on the twisted-pair-line way only for one.
[Claim 3] It is the signal-transmission system which has the signal-transmission track which connects electrically the logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit and a receiver circuit, and said driver circuit and said receiver circuit, and the power source and the grand pair transmission line of an electric power supply line, and is characterized by what the characteristic impedance of said power source and grand pair transmission line is equal to the sum total parallel impedance of the characteristic impedance of the transmission line of the number of signal driver circuits which hangs down from said power source and grand pair transmission line, or is been a value smaller than it.
[Claim 4] The logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit, and a receiver circuit, It has the signal-transmission track which connects said driver circuit and said receiver circuit electrically. Said signal-transmission track is a twisted-pair-line way altogether from the transistor outlet of said driver circuit to the inlet port of the transistor of said receiver circuit which should be joined. It is the signal-transmission system which considers only wiring which approaches the transistor contact section geometrically as stand-alone wiring, and is characterized by what said stand-alone wiring is the die length below a gate arrangement pitch.
[Claim 5] The logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit, and a receiver circuit, It has the signal-transmission track which connects said driver circuit and said receiver circuit electrically. The characteristic impedance adjusts said all signal-transmission tracks from the outlet of the transistor of the sending end by which the differential output was carried out from said driver circuit to the inlet port of the transistor of the termination of said receiver circuit. The interlayer connection column which is the structure where the terminator adjusted to termination was connected, and cannot adjust a

characteristic impedance, The connection of a beer hall and a connection stud is a signal-transmission system characterized by what it has the relation of tr>7tpd and tf>7tpd for, when the electromagnetic wave time delay of the discontinuous part of said connection is set to tpd and it sets tr and falling time amount to tf for pulse rise time.

[Claim 6] The logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit, and a receiver circuit, The signal-transmission track which connects said driver circuit and said receiver circuit electrically, It has the power source and the grand pair transmission line of an electric power supply line, and said all signal-transmission tracks, and said power source and grand pair transmission line are the structures where the TEM mode is maintained. The signal-transmission system characterized by what the structure where coating of the high dielectric constant ingredient which the effective dielectric constant of the part from which said electromagnetic wave leaks if it is in the structure where an electromagnetic wave leaks into air adjusts in an internal dielectric dielectric constant is carried out is included for.

[Claim 7] The logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit, and a receiver circuit, It has the signal-transmission track which connects said driver circuit and said receiver circuit electrically. Said signal-transmission track is a PEAKO planar track, a stack TOPEA track, a guard stack TOPEA track, or a GADOKO planar track, and the distance with a contiguity twisted-pair-line way is based on the own tooth space of a twisted-pair-line way. It is the signal-transmission system which said PEAKO planar track and said stack TOPEA track have a twice [more than] as many tooth space as this, and is characterized by what said guard stack TOPEA track and said GADOKO planar track have a tooth space of 1 time or more for.

[Claim 8] the time of said driver circuit and said receiver circuit consisting of two or more bits in a signal-transmission system according to claim 1 -- the whole-line way of said signal-transmission track -- crossing -- the physical structure -- relative -- the same -- etc. -- long -- a wire length -- ** -- it carries out and parallel -- etc. -- the signal-transmission system characterized by what is considered as radii-like wiring in order to consider as merits [wiring / fan-out] on the basis of long wiring, while and.

[Claim 9] The logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit, and a receiver circuit, It has the signal-transmission track which connects said driver circuit and said receiver circuit electrically. Said driver circuit and said receiver circuit Si or the n channel MOS of SiGe, In the bus switching circuit which does not have grounding at the n channel MES of GaAs A substantial differential output and a difference input circuit, Or the signal-transmission system characterized by what consisted of a reversal input nMOS differential current switching circuit, a constant current mold bus switching circuit, or a SHOTOKI high-speed bipolar differential circuit with a varactor.

[Claim 10] The signal-transmission system characterized by what is been the configuration which has the signal-transmission track which connects electrically the logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit and a receiver circuit, and said driver circuit and said receiver circuit, and has arranged the varactor of the same MOS, MES, or bipolar transistor structure complementary to said all transistors.

[Claim 11] It is the signal-transmission system which has the signal-transmission track which connects electrically the logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit and a receiver circuit, and said driver circuit and said receiver circuit, and will be characterized by the thing which uses said complementary transistor of each other as a complementary varactor, and which it is a configuration if said receiver circuit is a complementary transistor which a reversal signal or a clock inputs, and which approached.

[Claim 12] It is the signal-transmission system which it has the signal-transmission track which connects electrically the logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit and a receiver circuit, and said driver circuit and said receiver circuit, and said receiver circuit constitutes a differential-amplifier circuit, and is characterized by what all switch transistors are considered for as the configuration which holds a complementary varactor operation with a varactor or an of-the-same-kind reversal transistor.
[Claim 13] The logical circuit of a transistor over the whole electronic circuitry, the driver circuit included in a memory circuit, and a receiver circuit, It has the signal-transmission track which connects said driver circuit and said receiver circuit electrically. The flip-flop circuit of the preceding paragraph of said driver circuit is a circuit which outputs a reversal signal with a forward signal. It is the signal-transmission system characterized by what all switch transistors are considered for as the configuration which holds a complementary varactor operation with a varactor or an of-the-same-kind reversal transistor by considering as the circuit which makes a transistor configuration and a number of stages the same, and does not have the skew of both the signals output.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Affirming a conventional system configuration and a conventional bill of materials especially about a signal-transmission system, this invention is applied to the signal-transmission technique for letting a dozens of GHz band digital high speed signal pass, and relates to an effective technique.
[0002]
[Description of the Prior Art] According to the place which this invention person examined, the following techniques can be considered about a signal-transmission system.
[0003] Although the clock frequency for operating an LSI chip in recent years amounts to 1.5GHz, the frequency of the chip line wire way which exchanges this signal is in the condition that the highest also runs short of the bandwidths which do not pass to 530MHz but incorporate a signal to LSI to the demand of LSI. In order to make signal processing of LSI smooth, a logic chip or a memory chip also embeds cache memory, and supports the lack of a bandwidth.
[0004]
[Problem(s) to be Solved by the Invention] By the way, the following became clear as a result of this invention person's examining the above signal-transmission systems.
[0005] For example, as mentioned above, although cache memory is embedded and it corresponds to lack of a bandwidth, it not only needs the area of big cache memory, but address computation becomes excessive and architecture becomes complicated. If reservation of the clock of LSI and the adjusted I/O bandwidth can be performed, cache memory will be unnecessary and will serve as a simple system of architecture.
[0006] It must be the base of a digital system that it is essentially the same as the processing number of bits in a chip, and the clock of a chip and the transmission clock of an I/O bus of I/O of a chip must be the same as that of adjusting a bandwidth. From now on, it is in the time of rushing into a GHz band, and the improvement of a bus clock will be pressing need. Even if the transmission line which is the basic configuration of a bus has the property, it does not pass along a GHz band clock. GHz transmission can be performed only after preparation for all the package structures containing a driver receiver and it to let a high speed signal pass is made.
[0007] On the other hand, it is 2001 when the future in a chip is predicted. Symposium onVLSI The metal-oxide-semiconductor structure of 20nm of gate length is announced by Technology (2001. 6.Kyoto), and it is supposed that the digital signal which is 20GHz can be processed. It is predicted that it is realizable in 2007. It cannot let a 20-50GHz digital signal pass with wiring in a chip of 10mm angle, either. the system whole -- crossing -- uni--- the system construction which renewed the idea fundamentally is required to make it a FAI environment.
[0008] Then, the purpose of this invention is offering the signal-transmission technique for

letting the digital high speed signal of dozens of GHz band pass, affirming a conventional system configuration and a conventional bill of materials as much as possible.
[0009] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.
[0010]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0011] This invention is to make the configuration which eliminated the common power source of a common gland and a circuit, when a rough invention principle is expressed. Losing the break point when making it not restrict the process in which pulse-energy (the amount of charges) moves to a circuit or a track, as much as possible is called for at, and it causes reflection has pulse signal transmission of a GHz band. The result of having corresponded this faithfully serves as a concept of this invention.
[0012] Concretely, the signal-transmission system by this invention has the following descriptions.
[0013] (1) All (a driver and a receiver are included) of the logic of the transistor over the whole electronic circuitry, a memory circuit, etc. consider as a substantial difference input and a differential output, and they do not have distribution wiring. In a sending end side outgoing end (differential pair edge), it is circuitry which does not have any connection with a power source or a gland. A receiver receives by as a matter of fact detecting the potential difference of a qualitative differential signal.
[0014] (2) The electric power supply line of the above (1) is the structure used as a power source and a grand twisted-pair-line way, and is connected per 1 element circuit of each minimum logical element and a memory element circuit, and on the twisted-pair-line way only for one. In addition, the definition of a power source and the twisted-pair-line way only for grand 1 says the approach from the maximum contiguity bypass capacitor (advance base power source).
[0015] (3) The characteristic impedance of a power source and the grand pair transmission line is equal to the sum total parallel impedance of the transmission-line characteristic impedance of the number of signal drivers which hangs down from it, or is a value smaller than it.
[0016] (4) It is the transmission line (twisted-pair-line way) altogether from a transistor outlet to the inlet port of the transistor which should be joined, and although only wiring which approaches the transistor contact section geometrically is obliged to stand-alone wiring (independent wiring), this wiring is the die length below a gate arrangement pitch.
[0017] (5) All the transmission lines from the outlet (sending end) of the transistor outputted by differential are the structures where the terminator which the characteristic impedance adjusted to the inlet port of the transistor of termination, and was adjusted to termination was connected. The interlayer connection column which cannot adjust a characteristic impedance, a beer hall, a connection stud (bump), etc. have the relation of tr>7tpd and tf>7tpd, when tpd and pulse standup (falling) time amount are set to tr (tf) for the electromagnetic wave time delay of the discontinuous part. It is not this limitation when characteristic-impedance adjustment of an interlayer connection column, a beer hall, etc. is possible.
[0018] (6) All path cord ways (a signal-transmission track, a power source and a grand twisted-pair-line way) are the structures where the TEM mode is maintained. If it is in the structure where an electromagnetic wave leaks into air, the structure where coating of the high dielectric constant ingredient is carried out so that the effective dielectric constant of the part may have consistency in an internal dielectric dielectric constant is included.
[0019] (7) The transmission lines are a PEAKO planar, stack TOPEA, guard stack TOPEA, and GADOKO planar structure. In the tooth-space rule with a contiguity pair, a PEAKO planar and stack TOPEA have a twice [more than] as many tooth space as this on the basis of the

own tooth space of a twisted-pair-line way, and guard stack TOPEA and a GADOKO planar have a tooth space of 1 time or more.
[0020] (8) the time of the circuit of the above (1) consisting of two or more bits -- a whole-line way -- crossing -- the physical structure -- relative -- the same -- etc. -- long -- a wire length -- ** -- carry out. parallel -- etc. -- although based on long wiring, in order to consider as merits [wiring / fan-out], it considers as radii-like wiring.
[0021] (9) A driver receiver circuit consists of bus switching circuits which do not have grounding at the n channel MOS of Si or SiGe, and the n channel MES of GaAs in a substantial differential output, a difference input circuit (drawing 2), a reversal input nMOS differential current switching circuit (drawing 14), a constant current mold bus switching circuit (drawing 15), or a SHOTOKI high-speed bipolar differential circuit with a varactor (drawing 6).
[0022] (10) It is the configuration which has arranged the varactor of the same MOS, MES, and bipolar transistor structure complementary to all transistors.
[0023] (11) If it is the complementary transistor which a reversal signal or a clock inputs and which approached, it will consider as the configuration which uses them as a complementary varactor mutually.
[0024] (12) Although a receiver is characterized by the differential-amplifier circuit, consider all high-speed switch transistors as the configuration which holds a complementary varactor operation with a varactor or an of-the-same-kind reversal transistor.
[0025] (13) Although the flip-flop of the driver preceding paragraph is a circuit which outputs a reversal signal with a forward signal, let it be the circuit which makes a transistor configuration and a number of stages the same, and does not have the skew of both the signals output. Moreover, it considers as the same varactor configuration as the above (12) to a high-speed switch.
[0026]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the same member and explanation of the repeat is omitted.
[0027] As an example of the signal-transmission system in this invention, it explains in the gestalt of this operation in order of the I/O driver receiver circuitry of 1. LSI chip, and 2. system structure **.
[0028] 1. About I/O Driver Receiver Circuitry of I/O Driver Receiver Circuitry LSI Chip of LSI Chip P1 which this invention person already proposed before (JP,11-284126,A), Circuitry including the power source and grand pair structure of P2 (JP,2000-174505,A), The receiver circuit structure of P4 (JP,2001-211211,A), the transistor structure in which high speed signal processing of P9 (application for patent No. 315630 [2000 to]) is possible (reuse of an are recording carrier, such as varactor insertion), It becomes the configuration of having used preferably P12 (application for patent No. 369358 [2001 to]) which is the embedding bypass capacitor structures in a chip of P10 (application for patent No. 15753 [2002 to]), and those composition. About the part which overlaps said technique which this invention person proposed below, it is indicated as the proposal techniques P1, P2, P4, P9, P10, and P12, and detailed explanation is omitted.
[0029] First, if the circuit which exchanges the signal of the signal-transmission system in this invention is shown, it will become like drawing 2 mentioned later. It explains using drawing 2 for details. Here, the configuration of the driver and receiver which make a substantial differential output possible included in the logical circuit of a transistor over the whole electronic circuitry and a memory circuit is described. That there is no grounding in a sending end side differ as greatly as the former. Since the effectiveness of this invention cannot explain

clearly if you do not understand the phenomenon when operating at a high speed, an electromagnetism-concept is explained first.
[0030] Generally, a pulse is a synthetic wave including the higher harmonic of a sine wave. When the clock frequency of a pulse is made into a fundamental wave (70% of energy ****), it is composition of a 3 time higher harmonic with about 20% of energy, a 5 time higher harmonic with about 5% of energy, a 7 time higher harmonic with 1.5% of energy, a higher harmonic with 0.5% of energy, and the higher harmonic that has small energy by further odd times. If the higher harmonic which has a problem in energy is seen on an insurance side, the problem of a frequency high a single figure should be discussed to the clock frequency of a pulse. Moreover, it will be set to f= 0.35/tr or f= 0.35/tf, if it starts to the same pulse frequency, and the energy of a high order RF is so high that tr (falling tf) time amount is steep and a fundamental wave f is assumed from build up time. This is named a pulse effective frequency.
[0031] Resonance is caused to the transmission distance from which the sinusoidal energy transmitted at an electromagnetic wave rate serves as a turning point of a wave. The minimum turning point is quarter-wave length (lambda/4). Resonance of the above-mentioned high order higher harmonic will take place. If resonance takes place, the transfer conductance of the sine wave sets it infinity, and resistance is set to 0, and it will differ from the limited conductance of other sine waves greatly, and will transmit. That is, it means that it was amplified. It becomes the cause of electromagnetic radiation at the same time it transmits with the energy as a fundamental wave with the same higher harmonic with several% of energy and pulse shape is confused greatly, when extreme. Although this invention is the technique of the field of a digital circuit design, generally it is daring give this description in the knowledge of this viewpoint for the unacquainted field.
[0032] The above-mentioned 2001 Symposium on VLSI Even the 7 time higher harmonic of CPU announced by Technology and a 20GHz clock is made an issue of. It is a sine wave of 180GHz. Since the electromagnetic wave rate of the track which transmits the place of dielectric constant epsilonr=4 serves as 1.5x108 m/s, it is set to 180GHz lambda / 4= 21 micrometers. 21 micrometers or more cannot be made to crawl on the wire length in an LSI chip. A repeater circuit must be inserted when required. The wire length which poses a problem by RC delay also actually becomes less than [this], and all global wiring in an LSI chip must be made into the transmission line which can bear a higher harmonic.
[0033] As generalities of an LSI design, distribution of a wire length has become like drawing 1 . Drawing 1 is drawing showing wire-length distribution of general LSI (Japan Society for the Promotion of Science, the canonical structure electronic physical-properties 151st time [55th] committee study group, the committee [super-integration device system / 165th time / 16th / committee] research meeting said study group, guideline by value 1 ** of Tokyo Institute of Technology in 2000.7.19-20).
[0034] Long wiring is called so-called global wiring between functional block of LSI. It is proposed that the part (lumped-constant-circuit part) which does not have to be made into the transmission line, and the part (distributed constant circuit) which must be made into the transmission line are separated like drawing 1 . Also as for this invention, it is realistic to make it exist in the range of this proposal. It assumes that the circuitry which needs long wiring is 10% in LSI, and the countermeasures of problem generating in a RF, i.e., the technical contents of this invention, are explained below.
[0035] In order to acquire the output signal of the shape of a pulse of a driver, a switch and a power source are required. However, if it will be in the condition that a lot of currents flow in an instant from the condition that a current is not flowing, that current transition inclination di/dt will become steep, the sag of v=Ls (di/dt) will happen, and a power source Vdd will fall only for these v minutes in an instant (Vdd-v). A clock frequency's improving a single figure is that single figure v becomes large with the same wiring structure. If the parasitism inductance Ls in

a circuit is estimated, it will be set to 10pH by wiring die length of 10 micrometers. Conventionally, supposing it is the circuit which ******(ed) 10pH, for raising a frequency a single figure, 1pH, i.e., wiring die length, must be set to 1 micrometer. Although it must be made Ls=0.1pH or a current must be made regularity in order to maintain 10-micrometer wiring, in a lumped-constant-circuit-design, it is absolutely impossible. However, this serves as a possible thing in a distributed constant circuit. Here, it thinks in a concrete circuit.

[0036] When it is made less than [of a GHz band / signal standup tr=10ps], it does not operate at all conventionally in a circuit. The current switch mold driver which used the ECL circuit which is already historied is for eliminating this problem. However, this does not make business at all, either. The circuit of drawing 2 is a bus switching circuit made instead of ECL in one step of nMOS. Drawing 2 is drawing showing an example of structure which connects a receiver with a driver. Drawing 2 shows the driver 1 and receiver 2 which make a substantial differential output possible. A driver 1 consists of the nMOS transistors Tn1 and Tn3, varactors Vn2 and Vn4, resistance Re1 and Re2, etc., and the difference input signal Vsignal and /Vsignal (/ expresses a reversal signal) are supplied from a flip-flop. Moreover, the bypass capacitor Cb1 is connected with another driver etc. in common at the driver 1. A driver 1 is connected to a receiver 2 through a power source and the grand transmission line 4 at a power source Vdd through the signal-transmission track 3, respectively. Moreover, resistance Rt1 is connected to a receiver's 2 input edge.

[0037] Usually, a latch exists and the preceding paragraph of a driver 1 is a flip-flop circuit. Since this circuit has a differential output edge inevitably, the input signal to a driver 1 is nMOS arranged complementary, and can make comparatively easily the varactor insertion circuit shown in the proposal technique P9. Pn junction capacity of number of transistors increases, and the circuit which has arranged many transistors needs to make this discharge at the time of a signal change, and many superimposed instantaneous carrying current will not only be passed, but it induces the delay of switching operation. The driver circuit which prevents this must consist of minimum transistor counts like drawing 2 . The diffused resistor which becomes the cause which induces pn junction capacity has [the resistance Re1 and Re2 which led to the serial at these nMOS transistors Tn1 and Tn3] desirable metal membrane resistance of a tungsten or molybdenum, its silicide, etc. without using it.

[0038] The usefulness of this circuit is checked in simulation. It is drawing in which drawing 3 shows the simulation model circuit of a 35GHz clock, and drawing 4 shows the simulation result (upper case: a current, interruption:supply voltage, signal wave forms of a lower-berth:sending end and termination) of the circuit of drawing 3 , respectively.

[0039] In the driver circuit of this invention in tr=tf=10ps (an equivalent for a 35GHz clock frequency), drawing 3 set it as supply voltage Vdd=2V and the transmission line voltage of 100mV. Since the gland is a gland absolutely and does not serve as a substantial differential circuit like said drawing 2 , the simulator is carrying out the work which floats a gland. The simulation result is shown in drawing 4 . R3 and R4 add 800 ohms of current control resistance, and 100 ohms of transistor on resistance. U1, and U2, U3 and U4 express switching of a differential transistor. They are 0.001 ohms of on resistance, and 1 M omega of off resistance. In order to set up transistor parasitic capacitance, 5fF(s) of C3 and C4 were put side by side. T3 and the transmission line of T four considered as the characteristic impedance of 100 ohms (50ohms of one side) controllable within LSI considered to be suitable, and delay 20ps which 3mm track length deserves on the track surrounded with the insulating material of dielectric constant epsilonr=4 was set up. When a pair was constructed on the two tracks, it was set to 100 ohms, and by the simulator, since it was not able to do, two coaxial cables were used.

[0040] Naturally, although the terminator of R1 and R2 was 100ohms, the gate capacitance of 5fF(s) of C5 and C6 was added, respectively noting that it was inputted into the differential

gate. The characteristic impedance of the power source and grand twisted-pair-line way of T1 and T2 was made the same as a signal-line dimension, it was set as 100 ohms, and broke up in the chip, and the bypass capacitor of ** **** C1 and C2 was set to 100fF(s). Here, L1 and L2 were difficult and they set to reduce from the complexity of character top current pass called a confrontation electrode with the parasitism inductance of a bypass capacitor to 10pH. Although the differential signal was dealt with in single end like said drawing 2 , it was simulation, and since there was such no tool, it was expressed as the transmission line with two pairs of opposite glands.

[0041] Although the signal-level amplitude was very as low as 100mV, in differential I/O, it was presupposed that it is the detectable potential difference. Although constant current will always be passed to the terminator of the transmission line, the current is made small and it becomes a setup which was conscious of low power. In this setup, it is set to 2mA at the time of ON, and becomes consumption of 100 microwatts per one driver (at the time of ON). It is big power consumption relatively and it comes out inevitably as a guideline to consider as global wiring of the design stopped to about 10% per LSI. However, this is not the limitation of this invention.

[0042] In simulation, constant current is mostly maintained also with such high frequency, and it is almost satisfactory. Peak increase of a current is extent out of which depends on the deviation of the complementary property of the switch property in opening and a closing switching circuit, and this current indent comes for a while by the capacity of a receiving end. Since simulation of the varactor technique of the proposal technique P9 cannot be performed, when it has this, it should start and should serve as a wave steeper [falling] and beautiful. This is the big point of this invention. the same well -- for an inner reason, it is expected that a property cannot become imbalance easily and it will become a flat current.

[0043] By this, the circuit which can operate on the pulse effective frequency of 35GHz is able to be proposed. When it carries out based on drawing 2 R> 2 mentioned above and collects, (1) differential driver consists of one step of transistors, It is in structure. (2) -- the well with respectively same the transistor Tn1 by the side of a power source, a varactor Vn2 and a transistor Tn3, and a varactor Vn4 -- It is the structure which can perform charge exchange of all transistor capacity including a transistor diffusion capacitance, (3) A power source and a gland being the pair transmission lines and (4) differential signals are dealt with with single end-transmission-line structure (drawing 2), and it is the configuration which is not the differential on the basis of a general gland. It is the structure of specifying the gland not being arranged around the transmission line, (5) The differential pair signal is not connected to a gland or a power source from a driver outgoing end to a receiver input edge in any places, (6) It is the configuration which makes adjustment termination the same value as the characteristic impedance of the single end transmission line, (7) When a differential driver is BAIPORA, it is made the base, and being [it / the configuration of having considered the complementary use by the reversal signal of internal stored charge] ** becomes the proposal technique of this invention of the driver circumference. The above is an item guessed from drawing 2 , and is not all these proposals.

[0044] Next, if an example of transistor cross-section structure which realizes an operation of the above (2) is indicated, it will become like drawing 5 . Drawing 5 is drawing showing an example of the cross-section structure of the driver of the nMOS structure in drawing 2 mentioned above. The nMOS transistor Tn1 and a varactor Vn2 are in the structure of the P same wells 11, and consist of the gates G which sandwiched the source connected with n diffusion field 12 and the drain, and the oxide film 13. Similarly, the nMOS transistor Tn3 and a varactor Vn4 are in the structure of the P same wells 11, and consist of the gates G which sandwiched the source connected with n diffusion field 12 and the drain, and the oxide film 13. Signal Din is inputted into the gate G of the nMOS transistors Tn1 and Tn3, and a signal/Din is inputted into the gate of varactors Vn2 and Vn4.

[0045] thus, the nMOS transistors Tn1 and Tn3 and varactors Vn2 and Vn4 of a driver 1 are the same -- a well -- it is in structure. When the channel charge (a high hole consistency is temporarily called a channel although an electron 14 is a minority carrier in nMOS, and a hole 15 cannot be said to be a channel by the majority carrier) drawn close by each gate potential is wide opened with a complementary input signal, it is a time of suction of a contiguity transistor taking place, and high-speed carrier exchange can be performed. Moreover, it contributes also to saving of the power by reuse of a charge greatly.
[0046] If this is considered by the bipolar transistor, it will become cross-section structure like drawing 6 . Drawing 6 is drawing showing the carrier reuse circuit of a bipolar transistor. in addition, drawing 6 -- setting -- P -- n on a well 21 -- only the pnp transistor for glands formed into the structure of a well 22 is shown, and the pnp transistor for signal lines is omitting. In the carrier reuse circuit of a bipolar transistor, while the drawing by the side of the collector of the are recording minority carrier of the base is emphasized with a common collector current, a common collector compensates the complementary change in a depletion-layer charge. Although there is the drawing of an emitter than the effectiveness in MOS since it is not different from the former, it is the structure which makes big high-speed operation possible, and power can also be reduced by charge reuse. [less]
[0047] Next, an example of a receiver circuit is shown in drawing 7 . Drawing 7 is drawing showing an example of the circuit of a receiver edge. The receiver 2 of a substantial difference input consists of the differential amplifier section which consists of varactors ****11 and ****12, pMOS transistors Tp11 and Tp12, and nMOS transistors Tn11-Tn13, and the current setting section which consists of a pMOS transistor Tp13 and a nMOS transistor Tn14. the nMOS transistors Tn11 and Tn12 are common like drawing 5 and drawing 6 which were mentioned above because of a reversal signal input -- a well -- if structure and common collector structure are taken (when BAIPORA is adopted), high-speed operation is possible. A circuit is conventionally enough as the nMOS transistors Tn13 and Tn14 and the pMOS transistor Tp13 because of a static transistor. High-speed operation and power-saving actuation are attained now that what is necessary is just to make varactors ****11 and ****12 a set like said drawing 5 like said drawing 2 using reversal actuation of the nMOS transistors Tn11 and Tn12. the well with same pMOS transistor Tp11, a varactor **** 11 and the pMOS transistor Tp12, and Varactor **** 12 -- what is necessary is just to be in structure
[0048] Then, wiring structure is shown in drawing 8 . Drawing 8 is drawing showing an example of the planar structure of a driver. Like said drawing 2 , a driver consists of two nMOS transistors (Tn1, Tn3) and two varactors (Vn2, Vn4), and is formed into the structure of P wells 11. Gate G is connected with the pair transmission line 31 of an input signal, and the source and n diffusion field 12 of a drain are connected to the track which leads to a power source and a gland through contact 32, or the transmission line 33 of an output signal. The contact 35 to a right above layer connects with the transmission line 34 of a power source and a gland through resistance (Re1, Re2).
[0049] Thus, it is the important design point that input signals are [the pair transmission line 31 and the track of an output signal of the transmission line 33, and a power source and a grand pair] the transmission lines 34 (upper layer), and only wiring with which it never becomes a pair with geometric structure turns into the stand-alone wiring 36. In drawing 8 , the die length of this stand-alone wiring 36 is below 1 gate pitch, and makes it the range of a proposal technique to carry out wiring association in this way. the well with the same transistor which became a pair by the difference input -- it is also other important points that it is in structure. Here, each transmission line is a PEAKO planar track.
[0050] The power source and the grand layer are constructed by the 3rd layer as a PEAKO planar track along with each transistor array, as the two-dot chain line showed. It is drawing 9 which indicated that this was intelligible with cross-section structure. Drawing 9 is drawing

showing an example of the cross-section structure (cross-section notation abbreviation of an insulating layer) of the part of the transistor of a driver. It connects with the contact wiring 43 which leads to the upper wiring layer 42 through a plug 41 in one side, and n diffusion field 12 of a transistor is connected to an up power source and the grand pair layer 46 through a plug 41, a beer hall 44, a column 45, etc. on the other hand. Moreover, a power source and the grand pair maximum upper layer 47 are arranged right above [of an up power source and the grand pair layer 46]. in addition -- these -- each -- a conductor -- a part and each conductor layer are surrounded by the insulating layer.

[0051] Dimension conditions present the same conditions as the proposal technique P12. First, the cross section of the KOPURENA track of an up power source and the grand pair layer 46 is observed. In order to strengthen coupling of a power source and a gland, aspect ratio t/w>=1.5 are desirable. It is for coupling with a power source and a gland becoming strong by increasing a confrontation side, and making the leakage by the exterior of electromagnetic field small. Next, it is necessary to fulfill the conditions of d<h. It is to make it the fringe of confrontation side electromagnetic field not cross, namely, to avoid a cross talk over a layer, if possible. It is making it the 3rd s/d>=1.5. It is for this also avoiding the effect of a fringe. The same thing should be realized on all the PEAKO planar tracks (a signal line, clock line). As for all of the logic of LSI which operates with the clock frequency of several GHz or more, or the connection of a memory transistor, it is desirable to make it this structure as well as the structure of a driver 1 or a receiver 2. Of course, it cannot be overemphasized that this wiring Ruhr is preferably applied over all global wiring of a chip.

[0052] The output of a driver 1 is the process in which it results in a terminator through a principal ray way bus, and let it be the proposal range of this invention for the twisted-pair-line way of a grand level to exist as a grand line which connected and became independent to the common gland in any locations. A grand level carries out the swing jazz of the effectiveness by this to a pair signal line complementary, and it is to obtain maximum amplitude effective in the receiver 2 of the differential amplifier. Turbulence of the electromagnetic field of the transmission line becomes min, and the further effectiveness serves as a circuit which makes a parasitism inductance and parasitism capacitance min while a wave is not confused.

[0053] If the structure of the transmission line is shown, it will become like drawing 10 . drawing 10 is drawing showing an example of the suitable transmission line, in a PEAKO planar track and (b), a GADOKO planar track (both ends -- common) and (c) show a stack TOPEA track, and (d) shows [(a)] a guard stack TOPEA track (the upper and lower sides -- common), respectively. In drawing 10 , although it has described two pairs of transmission lines 51 at a time in an insulating layer 52, it is the Ruhr of a PEAKO planar and stack TOPEA that the distance with a contiguity twisted-pair-line way has a twice [more than] as many tooth space as this on the basis of the own tooth space of a twisted-pair-line way. A GADOKO planar track and a guard stack TOPEA track can design a contiguity wiring tooth space in the tooth space of 1 time or more on the basis of the own tooth space of a twisted-pair-line way. Let this limit be the proposal range of this invention. Although the advantage of a track with a guard is not this range, it can lower the impedance of the transmission line and can make it the suitable design range. In order to keep TEM wave transmission conditions, the transmission line 51 must be surrounded by the insulating layer 52 of a homogeneous insulating material. the range -- a PEAKO planar and stack TOPEA -- a conductor -- it is the breadth for 2s from a periphery, and let it to be the breadth of s be the proposal range of this invention in a GADOKO planar and stack TOPEA.

[0054] Countermeasures when breadth of this insulating layer 52 cannot be protected are proposed by drawing 11 . a conductor [in / in drawing 11 / a heterogeneity insulating layer] -- it is drawing showing an example of adjustment of the effective specific inductive capacity of a surrounding insulating layer. An example of a stack TOPEA track is shown in drawing 11 . This

image is a printed wired board and is the part of the solder resist 53 of the maximum upper layer. In order that the line of electric force which spreads in the upper part since the solder resist 53 is thin (thinner than 2s) may attain to the part of an air space, the effective specific inductive capacity of a solder resist 53 becomes small. If specific inductive capacity of the lower insulating layer 52 is set to a, this invention will make the proposal range the configuration which enlarges the dielectric constant of a solder resist 53 so that effective specific inductive capacity of a solder resist 53 may be set to the same a. Thereby, the transmission line 51 can maintain TEM wave mode substantially. If it is in a PEAKO planar and a stack TOPEA track, when an insulating layer and an air space of a different kind are in the range for 2s, the layer structure which substantial specific inductive capacity is the range of the breadth, and adjusted so that it might become the same specific inductive capacity is the general technical range. On the GADOKO planar and the guard stack TOPEA track, the convention same in the range of breadth s shall be kept.

[0055] Next, as drawing 12 shows, consideration to the die length of the impedance mismatch of a column, a beer hall, etc. is carried out. Drawing 12 is drawing showing an example of the model of the die length of the impedance mismatch of a column, a beer hall, etc., (a) shows the condition that between a track 61 and tracks 62 is connected in the column 63 and the beer hall 64, and (b) shows the output wave (the 1-4th order [1-2nd]) over an input wave. If specific inductive capacity of the insulating layer in a chip is set to 3, electromagnetic wave transmission speed will be set to 1.73x108 [m/s], and the transmission lag of 100-micrometer track length will serve as 0.578ps(es). Since the pulse rise time of a principal ray way set up temporarily with 10ps(es), it can be interpreted as the following phenomena. Even if energy flows into a mismatch part, the return is 0.578x2=1.156ps, and is the time amount in which a 8.5 times round trip between 10ps(es) is possible. It reaches mostly into build up time in this both-way adjustment at a stable zone. Therefore, it will start and the wave stabilized by inner wave-like turbulence after a certain thing started will advance wiring after passing a mismatch part.

[0056] As shown in drawing 13 , it sees in energy. the mismatch [drawing 13] impedance on the basis of 50 ohms -- many -- it is drawing showing an example of the transmission coefficient of reflective [degree] energy. A 50ohm/ohm [200] mismatch also passes the energy which went through the time amount which three round trips (the 1-4th order) take 90%. Conclusively, this die length can be disregarded. That is, let tr>7tpd be the proposal range in this invention.

[0057] As for drawing 2 mentioned above, the current of a power source and a grand twisted-pair-line way was complementary. Although the bypass capacitor, the varactor equivalent to it, etc. was required in the circuit which a power-source current turns on and off to signal turning on and off, the driver to which a current flows on a power source and a grand twisted-pair-line way next is proposed. If this is shown, it will become like drawing 14 . Drawing 14 is drawing showing an example of the driver of a differential type. Driver 1a of drawing 14 is the example of a current switch, it consists of nMOS transistors Tn21, Tn22, Tn23, and Tn24 and resistance Re 21, and a fixed current flows to an input signal Vsignal and /Vsignal. a duty time -- turning on and off -- if the same, it will become twice as many power consumption as said drawing 2 . A bypass capacitor Cb21 just does the cure of transistor capacity and a penetration current for a fixed current.

[0058] In order for the nMOS transistor Tn21, and Tn22, Tn23 and Tn24 to work complementary, it is not necessary to become possible to use this as a complementary varactor, and to prepare a varactor specially like drawing 2 mentioned above about transistor capacity. the well same when the transistor of the same class which operates complementary approaches here -- structure of acquiring the effectiveness of a complementary varactor can be made into the general proposal range of this invention by taking the structure installed

inside. What is necessary will be for the duty of a bypass capacitor Cb21 to become light by this effectiveness, and to carry out only penetration current correspondence at the time of switching.

[0059] Since the drain electrical potential difference of the nMOS transistors Tn21 and Tn22 and the drain electrical potential difference of the nMOS transistors Tn23 and Tn24 serve as a vertical stage, it will differ, and on resistance will differ. However, when either of the nMOS transistors Tn23 and Tn24 turns on, a drain electrical-potential-difference and source electrical potential difference is also about 0V. Because, since signal energy (the amount of charges) advances as an electromagnetic wave toward a receiver's 2 load resistance Rt21, it is for not returning, as long as there is no reflection. Therefore, as for the nMOS transistors Tn23 and Tn24, on resistance may differ from the nMOS transistors Tn21 and Tn22 that there should just be effectiveness which absorbs reflective energy. It is having the characteristic impedance of a signal-transmission way, and an impedance at the time of the same ON preferably. Of course, this is not necessarily a best policy in order to enlarge transistor size.

[0060] Even if the nMOS transistors Tn21 and Tn22 turn into a pMOS transistor, it cannot be overemphasized that the principle of drawing 14 is applicable. pMOS transistors are it being later than a nMOS transistor and needing a big area, and its drawing 14 constituted only from a nMOS transistor is more advantageous.

[0061] It looks back upon the predominance of the driver 1 of drawing 2 mentioned above once again to driver 1a of the differential type of drawing 14 . Although drawing 2 has the fault which passes a steep step current, power can save only OFF time amount. In fact, the steep step current is the same as di/dt of the penetration current of drawing 14 , and the engine performance and need for a bypass capacitor are the same. In order to re-charge this bypass capacitor that carried out the discharge as early as possible, the characteristic impedance of another cure stated at the beginning and a power-source track must be made small. It is because it recovers by 1-exp (t/Z0C). Here, Z0 is [time amount and C of the characteristic impedance of a power source and a grand twisted-pair-line way and t] bypass capacitors.

[0062] Even if it is the circuit of drawing 14 , if the characteristic impedance of the transmission line 4 of a power source and a grand pair is not small, an electrical potential difference falls by Ohm's law from load impedance. therefore -- drawing 14 and the example of both configurations of drawing 2 -- < (supply voltage twisted-pair-line way characteristic impedance) (signal-line characteristic impedance) -- ** -- it becomes the conditions to say. It is as a result of drawing 4 which simulation when equal mentioned above, and, as for supply voltage, 5% of drop is shown. A power source and grand twisted-pair-line way characteristic-impedance Z0P must be taken as Z0P<Z0/n, if the driver set which hangs down from them is set to n.

[0063] The problem is a time of a parasitism inductance existing in the transmission line 4 of a power source and a gland. On the circuit conditions of drawing 3 mentioned above, although it is 0H, supposing this is 50pH, it will consider as the step current of 10ps(es) by 2mA, and supposing it allows v= 10mV of 10% of power-source drops with a signal amplitude of 100mV, 0.05 or less nHs will be obtained by count of v=Lxdi/dt=0.05nHx2mA/10ps=10mV. With the configuration of drawing 8 mentioned above, since the conditions of a power source and a grand pair are kept immediately near the driver, the conditions of 50 or less pH are kept.

[0064] When this design is impossible, a bypass capacitor must cover it. Although this parasitism inductance must be 50 or less pH, it is unrealizable by the mass capacitor with a complicated current path. This need capacity is calculated.

[0065] It carries out on condition that drawing 3 mentioned above. Although the time amount current tpd which charges Charge Q to the die length of 3mm of signal-transmission tracks continues flowing, it serves as 20ps(es) on condition that drawing 3 . Since 10fF(s) are attached to the load, Q=2mAx20ps+10fFx10mV=40.1fC is needed. In addition, since the junction capacitance of a driver is compensated with the varactor, there is no need for a count

here. a small capacity which will call it 40.1fCx10xn/30mV=134 fFxn, and calls 1 byte 1.1nF(s) also as n from the conditions which permit a voltage drop 10% to supply voltage 1V and the signal amplitude of 100mV -- it is -- n= -- it becomes the conditions from which some can also protect parasitism inductance 100pH. Therefore, it is solvable by either the power source and the grand twisted-pair-line way characteristic impedance or the bypass capacitor and juxtaposition. However, in long wiring of a package passage, since tpd increases sharply, this circuit can apply only the conditions which lower the characteristic impedance of a power source and a grand twisted-pair-line way.

[0066] The approach of making it current regularity is proposed to drawing 15 to drawing 2 mentioned above. Drawing 15 is drawing showing an example of the driver of the bus switch mold which fixed the current. Driver 1b consists of nMOS transistors Tn31, Tn32, Tn33, and Tn34 and resistance Re31 and Re32, and an input signal Vsignal and /Vsignal are inputted. When a bus transistor is OFF, the nMOS transistors Tn33 and Tn34 flow through resistance Rt31, and the current seen from the power source and the gland serves as fixed conditions. the well with respectively same the nMOS transistors Tn31 and Tn33 and the nMOS transistors Tn32 and Tn34 -- it enters into structure and a charge is reused. Since the complementary current of a power source and the grand pair transmission line 4 is secured to the 1st a different place from said drawing 2 , if the conditions which are Z0P<Z0/n are secured, the bypass capacitor Cb31 is unnecessary. That is, although power is 2-double-consumed, it can be said to be an ideal circuit from drawing 2 . One side of the transmission line has the advantage of drawing 2 and drawing 15 in a grand level, and the handling on a circuit is easy for it. That is, handling of a single end wave can be performed seemingly (in fact, this is also splendid differential transmission on signal transduction). However, dropping on a gland by the termination side is not doing. This point is a concept important for this invention.

[0067] As an example of the last of a circuit, a D type flip-flop is shown in drawing 16 . Drawing 16 is drawing showing an example of D mold high-speed flip-flop circuit, (a) shows a flip-flop circuit and (b) shows an inverter, respectively. This flip-flop circuit is a D type flip-flop by the inverter which synchronizes with a clock, and consists of the nMOS transistor Tn41 driven with Clock CLK, pMOS transistors Tp42, Tp44, Tp46, and Tp48 which constitute an inverter, nMOS transistors Tn43, Tn45, Tn47, and Tn49, etc. The inverter has at the detail composition which has the diode mold varactors Vd41 and Vd42, respectively as shown in (b). In order to make a logic number of stages the same, only the part of an output Dout is not an inverter but a buffer configuration. Although it is hard to make from p mold factice, if it is i mold factice's SOI structure, it can make satisfactory.

[0068] If the structure and the principle of operation of a diode varactor are shown, it will become like drawing 17 . Drawing 17 is drawing showing an example of CMOS structure with a diode varactor, and its charge transfer. In drawing 17 , diode (Vd41) consists of an n+ diffusion field 72 and a p diffusion field 73, and a depletion layer 74 is formed in the perimeter of p diffusion field 73 for while it was formed with the pMOS transistor into the structure of n wells 71. The diode (Vd42) of another side formed with the nMOS transistor into the structure of p wells 75 consists of a p+ diffusion field 76 and an n diffusion field 77, and a depletion layer 78 is formed in the perimeter of n diffusion field 77. In SOI, diode is built into p wells and n wells, respectively, and the junction capacitance of diode can reuse complementary as stored charge.

[0069] Global wiring of drawing 1 mentioned above is a circuit which carries out the signal exchange which made the bus the subject, and it means covering once the path over the circuit system (flip-flop), i.e., a latch, a driver, a receiver, and a latch (flip-flop) by the above explanation. A differential signal serves as a common gland with the isolated signal system with a subject. If the ratio to the LSI chip of this circuit is only about 10%, power consumption will be so much satisfactory. However, this invention does not impose this percentage limit.

However, the power consumption of a lumped-constant-circuit part, gate delay, and RC delay cannot be disregarded, either. Establishing the reuse means of stored charge like drawing 17 to the circuits of DRAM, SRAM, and all logic gates has an advantage larger than increase of a transistor count. Therefore, the proposal range of this invention is characterized by establishing the charge reuse means required about all circuits.
[0070] Above, the device of a driver receiver transmission system and the circuit-part were explained.
[0071] 2. Explain the structural part which constitutes a system structure, next the system in alignment with this purpose. the chip passage was imagined -- if an ideal form is shown first -- etc. -- it becomes the structure connected with long concurrency wiring in the pitch. This is shown in drawing 18 . Drawing 18 is drawing showing an example of the connection structure of the transmission line between chips, and the top view where (a) looked at the chip by fluoroscopy, and (b) are the sectional views in the b-b' cutting plane line of (a). Between a chip 101 and a chip 102, it becomes a one-way (one-way traffic) track on the basis of pad-pad connection. Although the terminator 103 is connected, a receiver edge is not asked even if it is in a chip, and it is out of a chip. In short, it is adjustment termination. Although between the pad-pad shows the transmission line, it cannot be overemphasized that it is the transmission line like drawing 5 which also mentioned the inside of a chip above.
[0072] Although the transmission-line structure where it was desirable within a chip was a KOPURENA track, since the longwise large cross-section structure of an aspect ratio can be taken neither by the package nor the printed wired board, a stack TOPEA track is desirable track structure here. If a chip is seen by fluoroscopy as shown in (a), it will result [from a driver 104] in the chip pad 105 through a KOPURENA track, and flip chip bonding will connect with a patchboard 106 here. It connects with each lower layer in the bottom beer hall of a pad of a flip chip, and the signal line 107, and the power source and the grand line 108 under which it goes below pad width of face lap in the shortest possible distance, and become like the cross-section structure of (b).
[0073] As for the lower layer of a pair, it is more desirable than line breadth w to take 1.2 to 1.5 times in order to prevent a gap of the stack upper and lower sides and the leakage by the lower layer of electromagnetic field. Although already stated, if the relation of a stack TOPEA track is shown, it must be <=(d+t) s [w<=s and]/2, d<=2h1, and d<=2h2. from a driver 104 -- etc. -- the receiver pad 109 was formed in the location and it is connected with the receiver 110. If this short wiring is also in a package and it is in a stack TOPEA track and a chip, it is desirable that it is a KOPURENA track. The track which goes [line / 108 / a power source, / grand] direct is set to the bottom of the stack TOPEA track of a signal line 107 so that it may understand with cross-section structure. It seems that it was already said that the bypass capacitor 111 is installed around a driver 104.
[0074] With such a configuration, requirements as shown in following drawing 19 from the pad array of a driver chip and a receiver chip come out. Drawing 19 is drawing showing an example of constraint of a chip pad array. In drawing 19 , the chip 121 of a controller and the chip 122 of memory are connected through the bus way 125 from each chip pad 123,124.
[0075] (1) You need to make it crawl on a stack TOPEA track in a pitch twice the pitch of a chip pad, and a pad needs to align the direction of a bus way, and in the shape of [which go direct] a straight line. (2) It becomes the structure which picks out a signal line from 1 train pad of a chip, and the constraint when combining with other sides becomes large. These two constraint will raise the big problem for a designer. When a chip area carries out shrink by amelioration, shrink also of the pad pitch must be carried out. When shrink of the wiring pitch is carried out by technical improvement of a printed wired board, shrink of the chip pad pitch must be carried out similarly. The amelioration timing of a driver (controller) chip and a memory chip differs, and a match condition stops being able to find it easily. Amelioration of the junction technique

which influences reliability most will be called for, and the shrink of a pad pitch is accompanied by difficulty.

[0076] For this reason, although temporary solution can be aimed at by using the LSI package as INTAPOZA, extension of a branching wire length as shown in drawing 2020 , and fan-out mold wiring structure are searched for. Drawing 20 is drawing showing an example of the fan-out wiring structure when using a package. In drawing 20 , the package 133 which mounted the chip 132 of a controller on the printed wired board 131, and the package 135 which mounted the chip 134 of memory are connected through the bus way 136. In each package 133,135, the chip pad 137,140 and the package pad 138,141 are connected through the fan-out wiring 139,142.

[0077] Even if the structural device which stores wiring extension in limit within the limits is made, the principle of ** length wiring collapses and a problem comes out of fan-out structure to synchronous arrival. If it designs so that the wiring width of face of the fan-out wiring 139,142 may spread, the problem that a characteristic impedance changes will also crop up. This invention is proposed also about such problem-solving structures.

[0078] In drawing 20 , for convenience, although it is not a stack TOPEA track-expression, the fan-out structure in a package also presupposes that it is also wiring on a printed wired board a stack TOPEA track. The track dimension of a printed wired board 131 is made more thickly than the fan-out wiring 139,142. And the dimension can set up freely by adjusting the angle of divergence of a fan-out. That is, since it designed independently of the pitch of the chip pad 137,140, it had become the mainstream of the existing technique to use a package. By the high speed signal system, it crosses to all tracks and it is called for that it is long wiring -- a characteristic impedance is the same. This term is the same as that of the proposal technique P12.

[0079] It thinks on the basis of the characteristic impedance of 28 ohms. Although the characteristic impedance was set to 100 ohms within the chip, 28 ohms was chosen in order to show that 100-ohm design is easy here and the design of the worst case is also possible. Here, when w= 200 micrometers and epsilonr=4.5, it is the characteristic-impedance approximate expression (HaraldA.Wheeler) (symbolic reference of drawing 18) of a stack TOPEA track.

[0080]

[Equation 1]

$$Z_0 = (377/\sqrt{\varepsilon_r})\ \{(w/d) + (1/\pi)\ln(4) + ((\varepsilon_r+1)/2\pi\varepsilon_r)$$
$$\ln(\pi\varepsilon_r(w/d) + 0.94)/2\} + \{((\varepsilon_r-1)/2\pi\varepsilon_r^2)\ln(\varepsilon_r^2/16)\}^{-1} \quad [\Omega]$$

[0081] since -- d= 39 micrometers can be found. Here, although a branching pad exists, the bus structure is the same to termination, and does not need to worry about the mismatching of a characteristic impedance. If premised on long wiring, such as concurrency, a pad pitch can be set to w / 2= 100 micrometers, and a present condition technique can design it. If thickness of h2 is set to 60 micrometers which is the criterion of PURIPUREGU of a printed wired board 131, it will become ideal layer structure.

[0082] On the other hand, it is necessary to design package wiring according to the pitch of the chip pad 137,140. Here, if the pitch of the chip pad 137,140 is set to 50 micrometers, w of stack TOPEA wiring on a package will be set to 100 micrometers. It is set to d= 19.5 micrometers from an upper type. Although it becomes a 28-ohm transmission-line design from the chip pad 137,140 to a terminator now, since the wiring die length of the fan-out wiring 139,142 differs, a work like drawing 21 is carried out. Drawing 21 is drawing showing an example of ** length fan-out wiring.

[0083] Although MIANDA wiring of zigzag meandering structure is well adopted as a well-known example of long wiring to fan-out wiring etc., since it becomes a complicated

transmission characteristic electromagnetic by the adjacent effect, it arranges so that it may be merits [radii] like drawing 21 . namely, the fan-out wiring 139 (142) which connects the chip pad 137 (140) and the package pad 138 (141) -- radii -- it is -- etc. -- smooth transmission is not only expected, but [since there is no bending reflection like MIANDA,] by making it merit, since the distance between contiguity wiring is also comparatively large and it can take, it becomes advantageous arrangement to a cross talk.

[0084] When the formula designed with geometric radii is built, according to drawing 22 , it is as follows. Drawing 22 is drawing showing an example of the model for fixing Radii AB and changing Bowstring AB. Bowstring AB=l1 is a slant range between outermost edge pads. It becomes the relational expression which finds out the radius OP which makes this a variable and sets Radii AB constant. Now if segment PC=r1-h1 and CO=h1, 2(l1/2) =r12 and h12 will be obtained, and theta1/2=tan-1 (l1/2h1) to radii AB=r 1theta1 [a radian] will be obtained. r1 can be found if h1 is suitably calculated from these formulas. Radii AB=r 1theta1 can calculate hx and rx from the distance lx between pads after a degree as fixed.

[0085]

[Equation 2]

$$\text{円弧AB(一定)} = \sqrt{rx^2-(lx/2)^2}\cdot\tan^{-1}(lx/2)\sqrt{rx^2-(lx/2)^2}$$

[0086] Of course, the high order curve (drawing 21) of an ellipse or arbitration is sufficient as Radii AB, and it becomes the proposal item of this invention that there is no rapid deflection.

[0087] Above, although the design technique considered as concurrency bus wiring is well used after omitting a package, carrying out direct continuation of the chip on a printed wired board and passing through fan-out wiring recently, although the structure proposal which used the package was shown, it is hard to make changing the distance d between the twisted pair lines according to line breadth w on the same substrate. Even if it makes, it will become cost quantity, and the connection reliability of the level difference part falls.

[0088] a degree -- a proposal is related with the structure of fixing distance d between the twisted pair lines, and changing line breadth w. This is shown in drawing 23 . Drawing 23 is drawing showing an example of track structure which fixes distance between the twisted pair lines and changes line breadth. The part of fan-out structure which connects the chip pad 151 and the package pad 152 is made into a microstrip line 153 (or strip line) like drawing 23 , and it proposes using a concurrency bus way properly as a stack TOPEA track 154. In addition, other parts of a microstrip line 153 serve as the solid gland 155, and the branching electrode 156 is formed in the stack TOPEA track 154 as an example.

[0089] Breadth and the capacitance C0 per unit length increase [electric field / as opposed to a gland in a microstrip line (strip line) 153]. Consequently, [0090]

[Equation 3]

$$Z_0 = \sqrt{L_0/C_0}$$

[0091] It will become small if it is the ** same line breadth w. On the contrary, Z0 can make fixed, then w small. The approximate expression (Harold A.Wheeler) (symbolic reference of drawing 18) of a microstrip line 153 is [0092].

[Equation 4]

$$Z_0 = (377/2.828\pi\sqrt{\varepsilon r+1})\ln\{1+(4d/w\ [((14+8/\varepsilon r)/11)(4d/w)+\sqrt{((14+8/\varepsilon r)/11)^2(4h/w)^2+\pi^2(1+1/\varepsilon r)/2]}\ )\}\ [\Omega]$$

[0093] It becomes. If Z0=28ohm, w= 170 micrometers will be computed by d= 39 micrometers. If the conductor thickness of t= 25 micrometers is amended, in order to subtract 25 micrometers experientially, w= 145 micrometers of amendments are obtained. If it is made a microstrip line 153 to w= 200 micrometers of stack TOPEA tracks at the d= 39 micrometers of

the same tooth spaces between the twisted pair lines, detailed-ization will be attained to w= 145 micrometers. An image becomes like drawing 23 R> 3.
[0094] To the design of a chip pad 50micrometer pitch and w= 100 micrometers of fan-out wiring, although it is insufficient, correspondence of 145 micrometers is attained by narrowing down near the pole of a pad. the idea as a branching wire length that the wire length to narrow down is the same -- good -- < (comprehensive time delay of 7x narrowing-down die length) (build up time) -- what is necessary is just to become
[0095] Finally, if the system of connection between chips, and a power source and grand distribution is shown, it will become like drawing 24 . Drawing 24 is drawing showing between packages the connection during the chip which in other words was mounted in each package, and an example of arrangement of a power source and a grand twisted-pair-line way. In the system shown in drawing 24 , although it understands lucidly, the solid gland and the solid power source are unnecessary only by establishing a power source and the grand common track 161, and it must not never prepare. Although the die length of the signal-line way of the signal bus 167 over the chip mounted in each of memory packages 163-166 from the CPU package 162 differs, it can synchronize, if the transmission lag of the clock signal supplied in the clock transmission line 168 is used. In addition, the power source to the CPU package 162 and memory packages 163-166 is supplied through the power-source twisted-pair-line way 170 in the I/O arrangement tooth space 169 from a power source and the grand common track 161.
[0096] As explained above, according to the signal-transmission system of the gestalt of this operation, it is the process in which change into delivery the charge supplied from the twisted-pair-line way of a power source and a gland, and the charge to which through and a receiving transistor were made to react to and the signal-transmission track was made to react further is duly changed into a transmitting transistor by the terminator at heat. A dozens of GHz signal needs to keep such a concept, and can let the digital high speed signal of dozens of GHz band pass by proposing the structure and the configuration which realize this concept, and its approach as mentioned above.
[0097] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of the operation, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.
[0098]
[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
[0099] the signal transmission technique for let the digital high speed signal of dozens of GHz band pass can be offer by lose the break point which make the configuration which eliminated the common power source of a common gland and a circuit, and it be make not to restrict the process in which pulse-energy (the amount of charges) move to a circuit or a track, as much as possible, and cause reflection according to this invention, affirm a conventional system configuration and a conventional bill of materials as much as possible.

[Translation done.]

* NOTICES *

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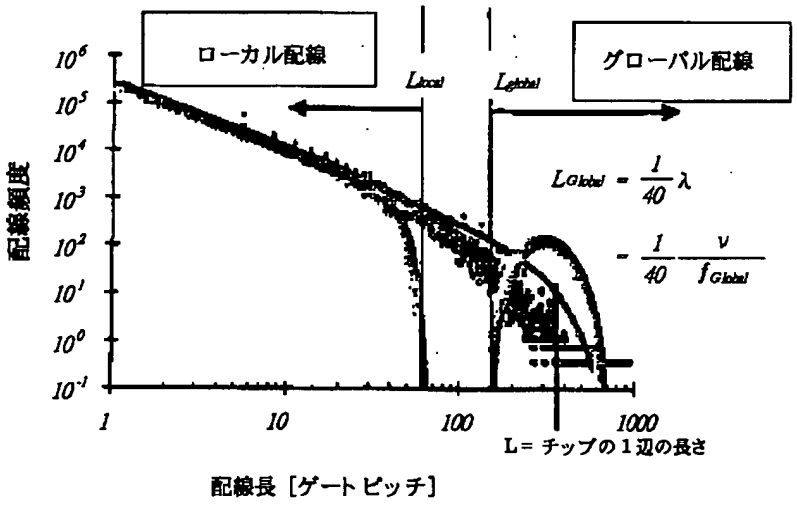
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

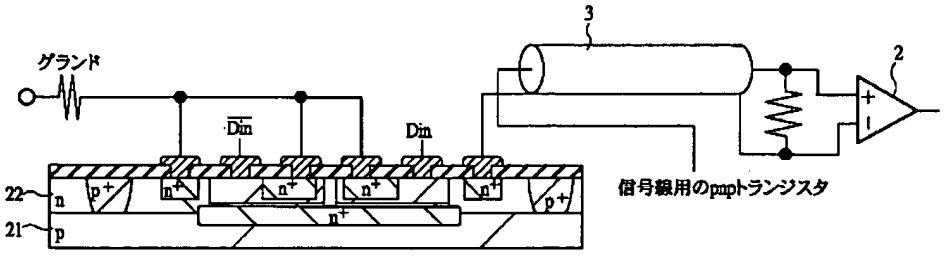
[Drawing 1]

図 1



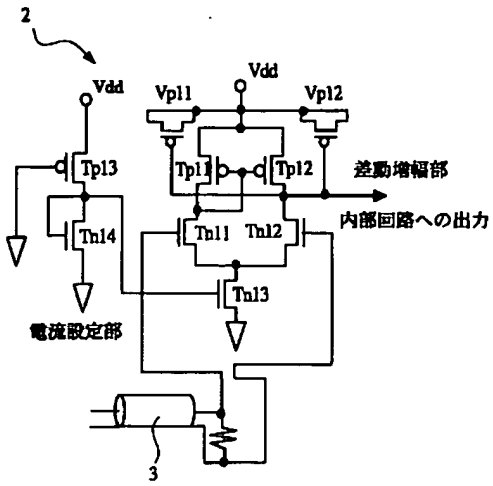
[Drawing 6]

図 6



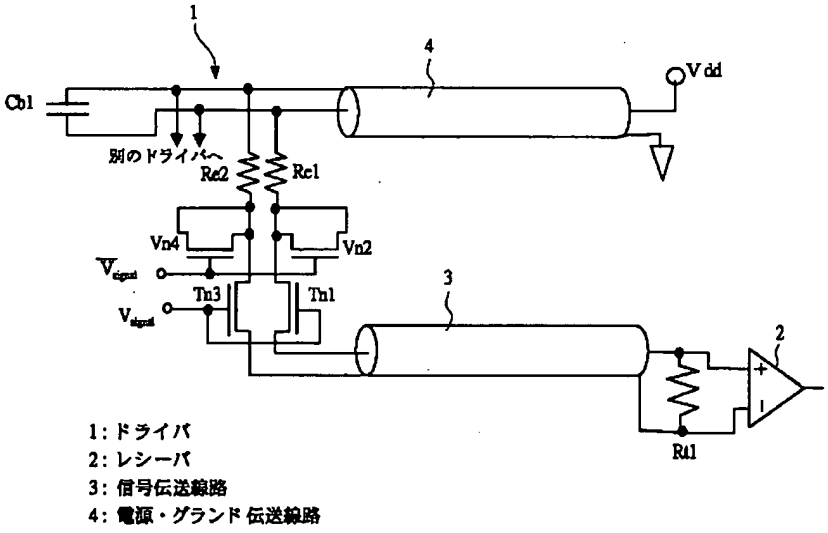
[Drawing 7]

図 7



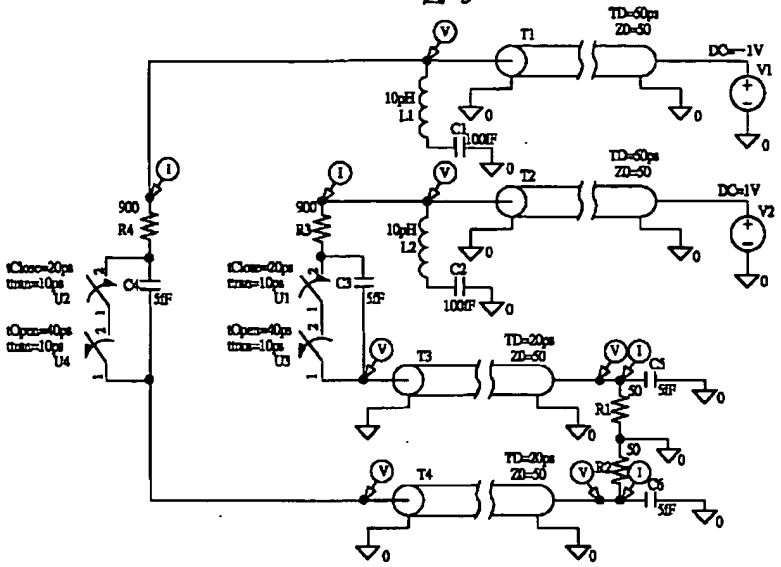
[Drawing 2]

図 2



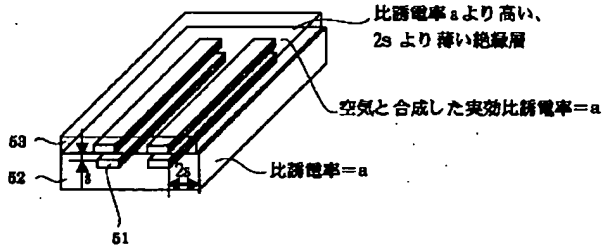
[Drawing 3]

図 3



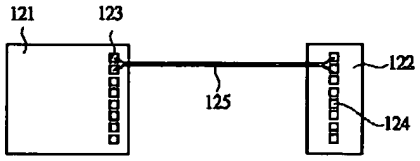
[Drawing 11]

図 11



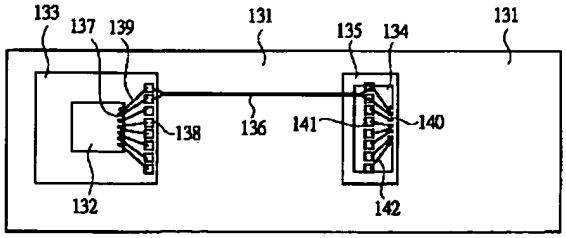
[Drawing 19]

図 19



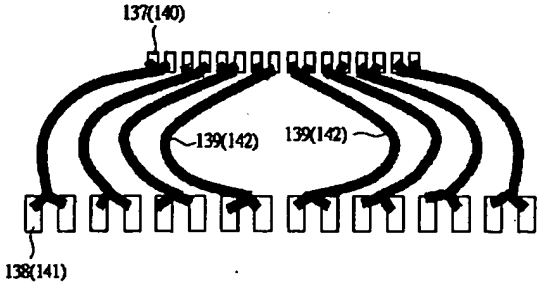
[Drawing 20]

図 20



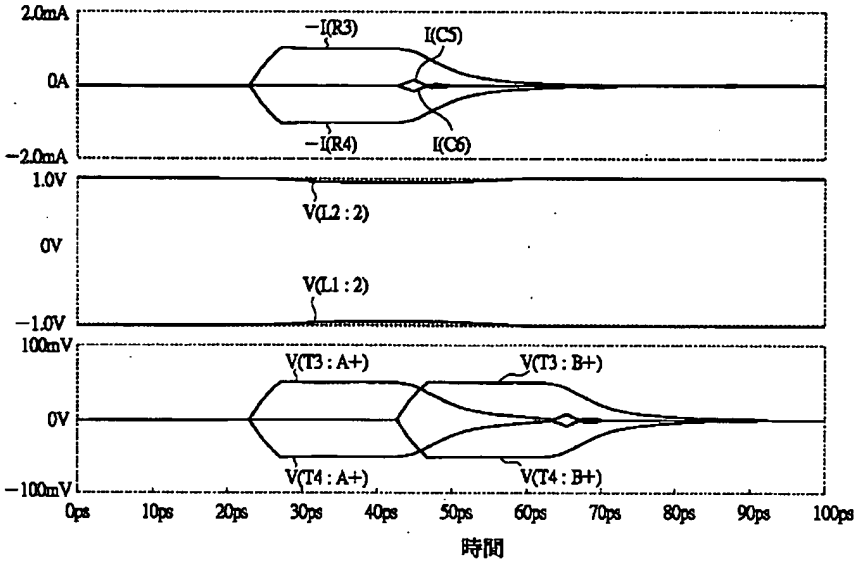
[Drawing 21]

図 21



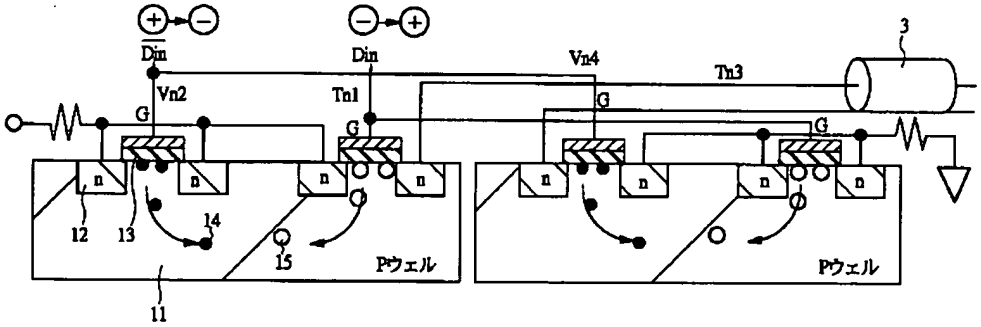
[Drawing 4]

図 4



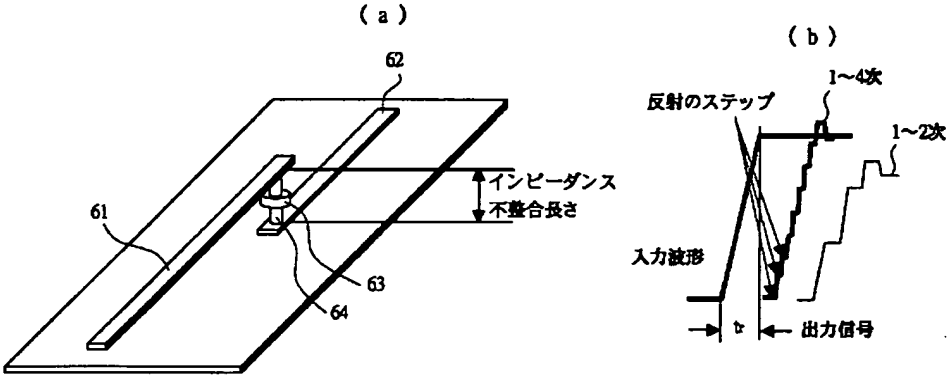
[Drawing 5]

図 5



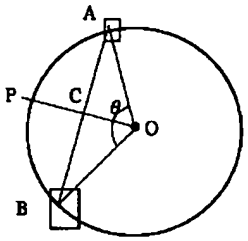
[Drawing 12]

図 12



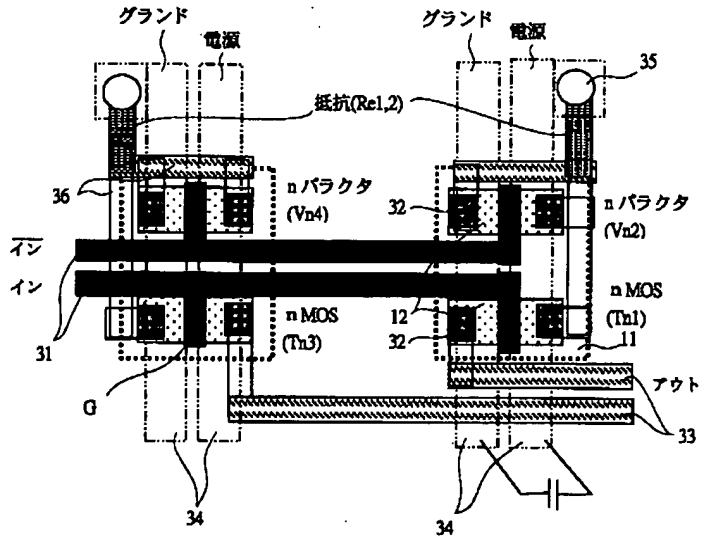
[Drawing 22]

図 22



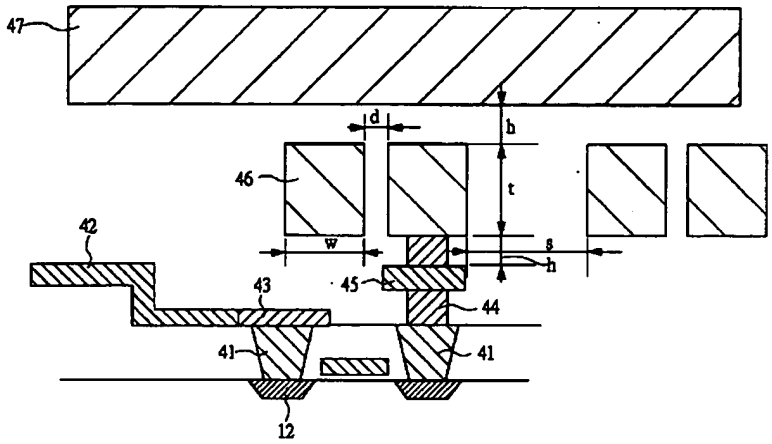
[Drawing 8]

図 8



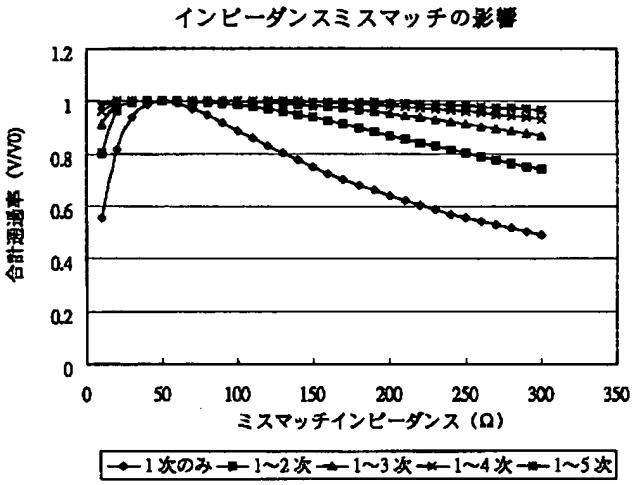
[Drawing 9]

図 9



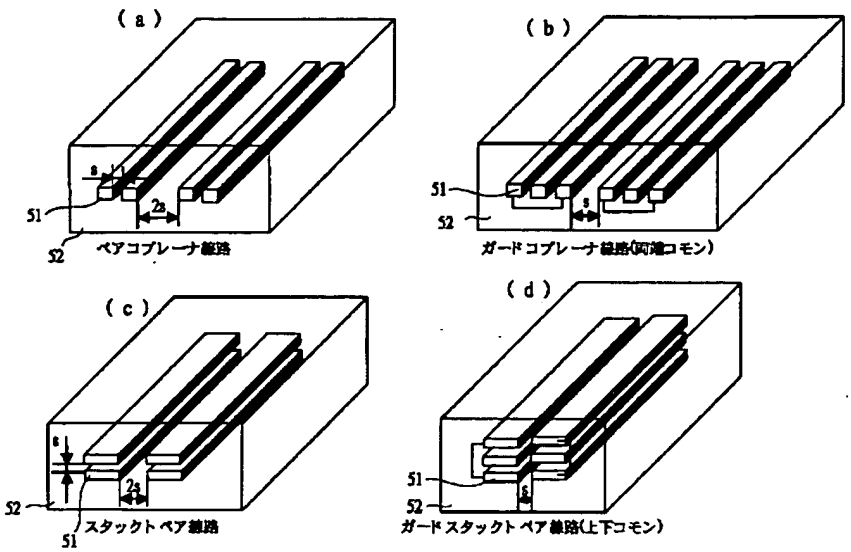
[Drawing 13]

図 13



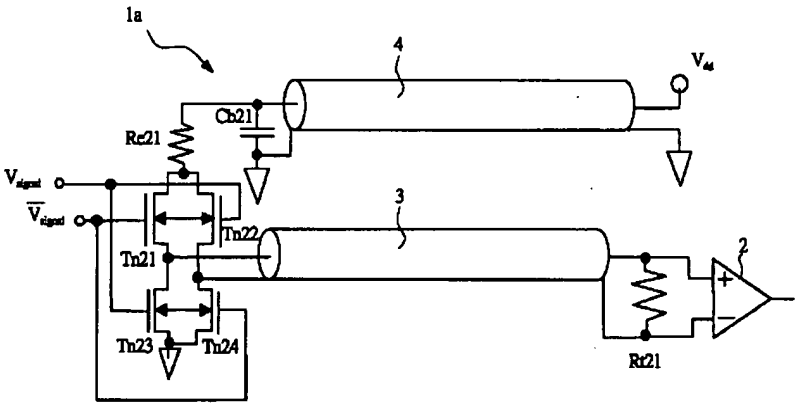
[Drawing 10]

図 10



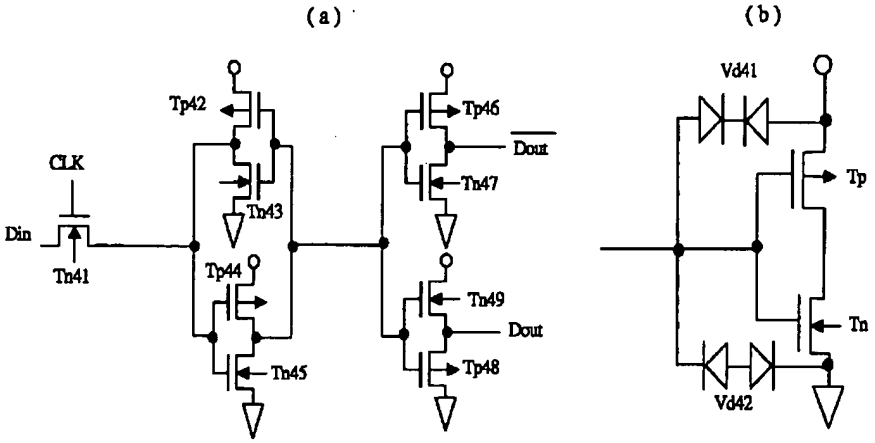
[Drawing 14]

図 14



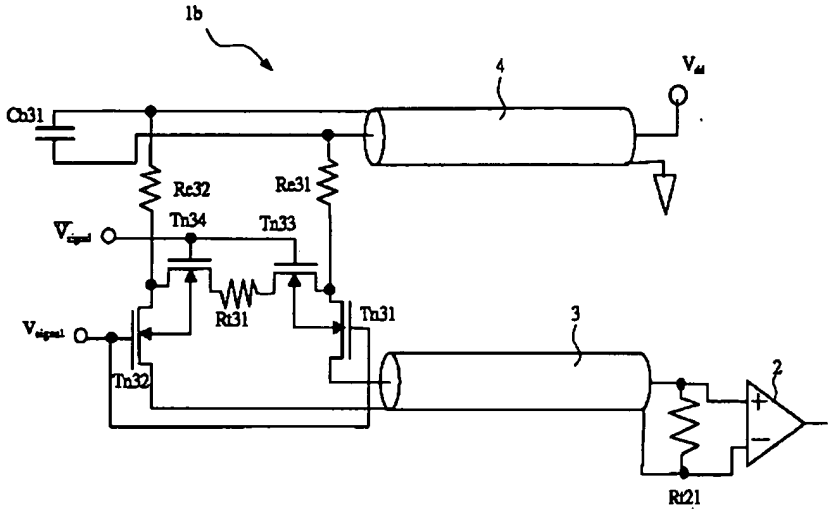
[Drawing 16]

図 16



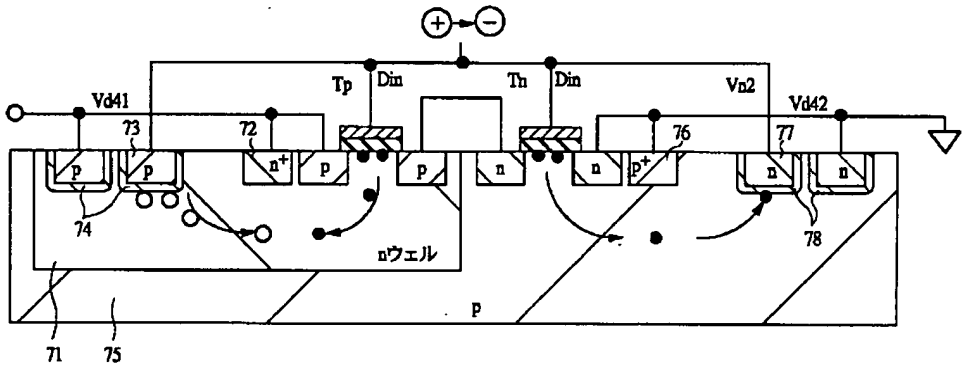
[Drawing 15]

図 15



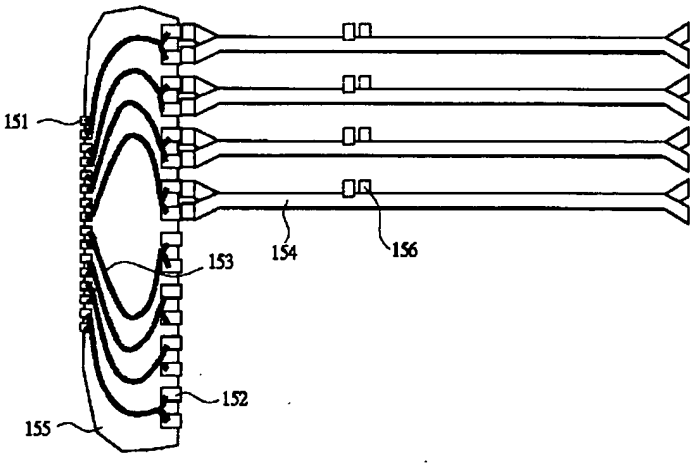
[Drawing 17]

図 17



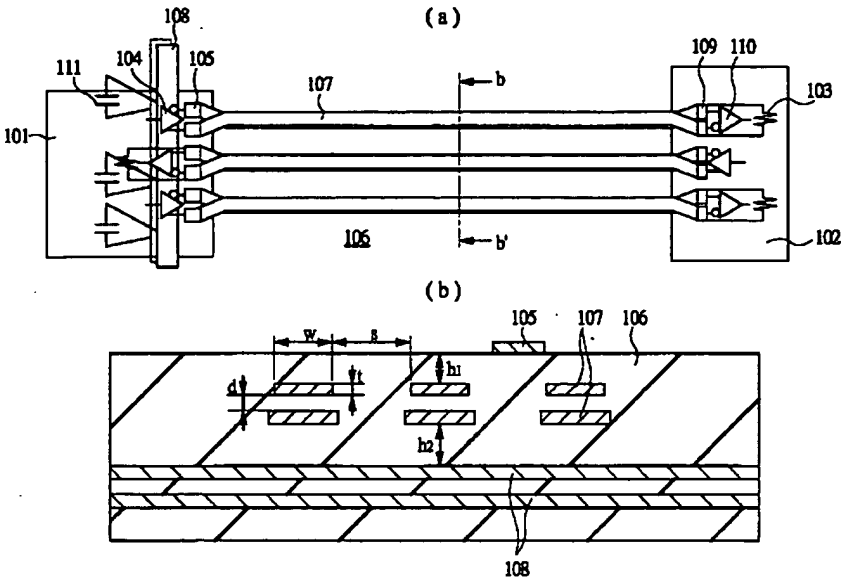
[Drawing 23]

図 23



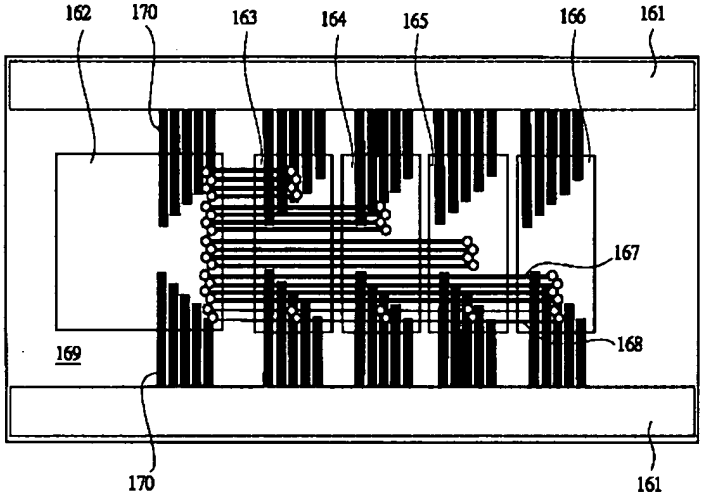
[Drawing 18]

図 18



[Drawing 24]

図 24



[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] In the gestalt of 1 operation of this invention, it is drawing showing wire-length distribution of general LSI.
[Drawing 2] In the gestalt of 1 operation of this invention, it is drawing showing an example of structure which connects a receiver with a driver.
[Drawing 3] In the gestalt of 1 operation of this invention, it is drawing showing the simulation model circuit of a 35GHz clock.
[Drawing 4] In the gestalt of 1 operation of this invention, it is drawing showing the simulation result of the circuit of drawing 3 .
[Drawing 5] In the gestalt of 1 operation of this invention, it is drawing showing an example of the cross-section structure of the driver of the nMOS structure in drawing 2 .
[Drawing 6] In the gestalt of 1 operation of this invention, it is drawing showing the carrier reuse circuit of a bipolar transistor.
[Drawing 7] In the gestalt of 1 operation of this invention, it is drawing showing an example of the circuit of a receiver edge.
[Drawing 8] In the gestalt of 1 operation of this invention, it is drawing showing an example of the planar structure of a driver.
[Drawing 9] In the gestalt of 1 operation of this invention, it is drawing showing an example of the cross-section structure of the part of the transistor of a driver.
[Drawing 10] (a) - (d) is drawing showing an example of the suitable transmission line in the gestalt of 1 operation of this invention.
[Drawing 11] a conductor [in / on the gestalt of 1 operation of this invention, and / a heterogeneity insulating layer] -- it is drawing showing an example of adjustment of the effective specific inductive capacity of a surrounding insulating layer.
[Drawing 12] (a) and (b) are drawings showing an example of the model of the die length of the impedance mismatch of a column, a beer hall, etc. in the gestalt of 1 operation of this invention.
[Drawing 13] the mismatch impedance on the basis of 50 ohms in the gestalt of 1 operation of this invention -- many -- it is drawing showing an example of the transmission coefficient of reflective [degree] energy.
[Drawing 14] In the gestalt of 1 operation of this invention, it is drawing showing an example of the driver of a differential type.
[Drawing 15] In the gestalt of 1 operation of this invention, it is drawing showing an example of the driver of the bus switch mold which fixed the current.
[Drawing 16] (a) and (b) are drawings showing an example of D mold high-speed flip-flop circuit in the gestalt of 1 operation of this invention.
[Drawing 17] In the gestalt of 1 operation of this invention, it is drawing showing an example of CMOS structure with a diode varactor, and its charge transfer.

[Drawing 18] (a) and (b) are drawings showing an example of the connection structure of the transmission line between chips in the gestalt of 1 operation of this invention.
[Drawing 19] In the gestalt of 1 operation of this invention, it is drawing showing an example of constraint of a chip pad array.
[Drawing 20] In the gestalt of 1 operation of this invention, it is drawing showing an example of the fan-out wiring structure when using a package.
[Drawing 21] the gestalt of 1 operation of this invention -- setting -- etc. -- it is drawing showing an example of long fan-out wiring.
[Drawing 22] In the gestalt of 1 operation of this invention, it is drawing showing an example of the model for fixing Radii AB and changing Bowstring AB.
[Drawing 23] In the gestalt of 1 operation of this invention, it is drawing showing an example of track structure which fixes distance between the twisted pair lines and changes line breadth.
[Drawing 24] In the gestalt of 1 operation of this invention, it is drawing showing an example of arrangement of connection between chips, and a power source and a grand twisted-pair-line way.
[Description of Notations]
1, 1a, 1b Driver
2 Receiver
3 Signal-Transmission Track
4 Power Source and Grand Transmission Line
11 P Wells
12 N Diffusion Field
13 Oxide Film
14 Electron
15 Hole
21 P Wells
22 N Wells
31 Pair Transmission Line
32 Contact
33 Transmission Line
34 Transmission Line
35 Contact
36 Stand-alone Wiring
41 Plug
42 The Upper Wiring Layer
43 Contact Wiring
44 Beer Hall
45 Column
46 Up Power Source and Grand Pair Layer
47 Power Source and Grand Pair Maximum Upper Layer
51 Transmission Line
52 Insulating Layer
53 Solder Resist
61 62 Track
63 Column
64 Beer Hall
71 N Wells
72 N+ Diffusion Field
73 P Diffusion Field
74 Depletion Layer

75 P Wells
76 P+ Diffusion Field
77 N Diffusion Field
78 Depletion Layer
101,102 Chip
103 Terminator
104 Driver
105 Chip Pad
106 Patchboard
107 Signal Line
108 Power Source and Grand Line
109 Receiver Pad
110 Receiver
111 Bypass Capacitor
121,122 Chip
123,124 Chip pad
125 Bus Way
131 Printed Wired Board
132,134 Chip
133,135 Package
136 Bus Way
137,140 Chip pad
138,141 Package pad
139,142 Fan-out wiring
151 Chip Pad
152 Package Pad
153 Microstrip Line
154 Stack TOPEA Track
155 Solid Gland
156 Branching Electrode
161 Power Source and Grand Common Track
162 CPU Package
163-166 Memory package
167 Signal Bus
168 Clock Transmission Line
169 I/O Arrangement Tooth Space
170 Power-Source Twisted-Pair-Line Way

[Translation done.]